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NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 06/16/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
JAIN, RAJ K	
ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 06/16/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,458	10/29/2003	Abbas Amirichimeh	1875.3640002/JTH/TAD	4577

TITLE OF INVENTION: CROSS LINK MULTIPLEXER BUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$0	$1440	$1440	09/16/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

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nonprovisional	NO	$1440	$0	$1440	$1440	09/16/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
JAIN, RAJ K	2616	370-304000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 868 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 868 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/695,458	AMIRICHIMEH ET AL.	
	Examiner	Art Unit	
	RAJ K. JAIN	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/18/08*.

2. ☒ The allowed claim(s) is/are *1-5, 7-13, 17-25, 29-35, 37, 39-43 renumbered 1-34*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/18/08
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Timothy Doyle on May 8, 2008.

Amend the following claims:

13. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a first cross link multiplexer with a destination port configured to receive a data signal and a second cross link multiplexer with an origin port configured to produce said data signal; and

a plurality of interconnects, wherein a first set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein a first interconnect of said first set of interconnects is configured to convey a first bit of a number of bits of said data signal in a first ~~direction and~~ direction, a second interconnect of said first set of interconnects is configured to convey a second bit of said number of bits of said data signal in said first ~~direction;~~ direction, and the first bit remains substantially synchronized with the second bit;

wherein said first cross link multiplexer is configured to convey said data signal toward said second cross link multiplexer in said first direction via said first set of interconnects coupled to a third cross link multiplexer of said plurality of cross link multiplexers and said first cross link multiplexer is configured to convey said data signal toward said second cross link multiplexer in a second direction via a second set of interconnects of said plurality of interconnects coupled other than to said third cross link multiplexer.

18. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a number of bits;

wherein at least one of said plurality of cross link multiplexers and said plurality of interconnects is configured so that a first bit of said number of ~~bits~~ bits, conveyed by a first interconnect of said plurality of interconnects, remains substantially synchronized with a second bit of said number of ~~bits;~~ bits, conveyed by a second interconnect of said plurality of interconnects;

wherein said plurality of cross link multiplexers is configured to delay conveyance of said first bit by a gate delay time;

wherein said plurality of interconnects is configured to delay conveyance of said second bit by a path delay time; and

wherein said gate delay time and said path delay time are set so that said first bit remains substantially synchronized with said second bit.

19. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a number of bits;

wherein at least one of said plurality of cross link multiplexers and said plurality of interconnects is configured so that a first bit of said number of ~~bits~~ bits, conveyed by a first interconnect of said plurality of interconnects, remains substantially synchronized with a second bit of said number of ~~bits;~~ bits, conveyed by a second interconnect of said plurality of interconnects; and

wherein a first cross link multiplexer of said plurality of cross link multiplexers is configured to process said signal formatted according to a first physical layer communications protocol and a second cross link multiplexer of said plurality of cross link multiplexers is configured to process said signal formatted according to a second physical layer communications protocol.

24. (Currently Amended) A method for conveying a data signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the data signal from a first cross link multiplexer of the cross link multiplexer bus via a second cross link multiplexer of the cross link multiplexer bus toward a third cross link multiplexer of the cross link multiplexer bus; and

(2) conveying the data signal from the first cross link multiplexer other than via the second cross link multiplexer toward the third cross link multiplexer;

wherein a first interconnect of a plurality of interconnects is used to convey a first bit of the data signal from the first cross link multiplexer to the second cross link ~~multiplexer and~~ multiplexer, a second interconnect of the plurality of interconnects is used to convey a second bit of the data signal from the first cross link multiplexer to the second cross link ~~multiplexer.~~ multiplexer, and the first bit remains substantially synchronized with the second bit.

30. (Currently Amended) A method for conveying, in parallel, bits of a character of a data signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying a first bit of the bits of the character of the data signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer ~~bus;~~ bus, wherein a first interconnect of a plurality of interconnects is used to convey the first bit from the first cross link multiplexer to the second cross link multiplexer;

(2) conveying a second bit of the bits of the character of the data signal from the first cross link multiplexer to the second cross link ~~multiplexer; and~~ multiplexer, wherein a second interconnect of the plurality of interconnects is used to convey the second bit from the first cross link multiplexer to the second cross link multiplexer; and

(3) delaying said conveyance of the first bit so that the first bit remains substantially synchronized with the second bit.

32. (Currently Amended) A method for conveying a data signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the data signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer ~~bus; and~~ bus, wherein a first interconnect of a plurality of interconnects is used to convey a first bit of the data signal from the first cross link multiplexer to the second cross link multiplexer and a second interconnect of the plurality of interconnects is used to convey a second bit of the data signal from the first cross link multiplexer to the second cross link multiplexer;

(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the data signal from a first format to a second ~~format;~~ format,

~~(3) synchronizing bits of a character of the signal;~~

wherein the first format is one of a 10 Gigabit Media Independent Interface protocol, a 10 Gigabit Attachment Unit Interface protocol, and a Converged Data Link protocol, the second format is one of the 10 Gigabit Media Independent Interface protocol, the 10 Gigabit Attachment Unit Interface protocol, and the Converged Data Link protocol, and the second format is different from the first ~~format.~~ format; and

(3) synchronizing the first bit with the second bit.

33. (Currently Amended) The method of claim 32, further comprising the step of:

(4) receiving the data signal at the first cross link multiplexer.

34. (Currently Amended) The method of claim 32, further comprising the step of:
(4) reconverting the data signal from the second format to the first format.

35. (Currently Amended) The method of claim 32, further comprising the step of:
(4) transmitting the data signal from the second cross link multiplexer.

37. (Currently Amended) A method for conveying a data signal across a cross link multiplexer bus, comprising the steps of:
(1) conveying the data signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer ~~bus;~~ bus, wherein a first interconnect of a plurality of interconnects is used to convey a first bit of the data signal from the first cross link multiplexer to the second cross link multiplexer and a second interconnect of the plurality of interconnects is used to convey a second bit of the data signal from the first cross link multiplexer to the second cross link multiplexer;
(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the data signal from a first format to a second format; and
(3) ~~synchronizing bits of a character of the signal;~~
~~wherein said synchronizing step comprises the step of~~ conveying each ~~bit~~ of the ~~bits~~ first bit and the second bit through a corresponding delay ~~flip-flop.~~ flip-flop to synchronize the first bit with the second bit.

39. (Currently Amended) A method for conveying a data signal across a cross link multiplexer bus, comprising the steps of:
(1) conveying the data signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer ~~bus;~~ bus, wherein a first interconnect of a plurality of interconnects is used to convey a first bit of the data signal from the first cross link multiplexer to the second cross link multiplexer and a second interconnect of the plurality of interconnects is used to convey a second bit of the data signal from the first cross link multiplexer to the second cross link multiplexer;
(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the data signal from a first format to a second ~~format; and~~ format, wherein the data signal is configured to be represented as a series of characters, a character of the series of characters is conveyed during one cycle of a clock that controls conveyance of the data signal, the first format has a first number of bits for data for a first character from the series of characters, the second format has a second number of bits for data for the first character and data for a second character from the series of characters, and the first number is different from the second number; and
(3) synchronizing ~~bits of a character of~~ the ~~signal;~~ first bit with the second bit.
~~wherein the signal is configured to be represented as a series of characters;~~
~~wherein one character of the series of characters is conveyed during one cycle of a clock that controls conveyance of the signal;~~

~~wherein the first format has a first number of bits for data for a first character from the series of characters; and~~

~~wherein the second format has a second number of bits for data for the first character and data for a second character from the series of characters.~~

41. (Currently Amended) In a cross link multiplexer bus configured to convey a data signal in which a character is represented by a first bit of the data signal and a second ~~bit,~~ bit of the data signal, a method for synchronizing the first bit and the second bit, comprising the steps of:

(1) determining a first time for the first bit of the data signal to be conveyed via a first interconnect from a first cross link multiplexer to a second cross link multiplexer when a first series of delay buffers is bypassed;

(2) determining a second time for the second bit of the data signal to be conveyed via a second interconnect from the first cross link multiplexer to the second cross link multiplexer when a second series of delay buffers is bypassed, the second time greater than the first time;

(3) determining a desired delay time for the first bit of the data signal so that the first bit of the data signal is synchronized with the second bit of the data signal; and

(4) aligning the first series of delay buffers to increase the first time by the desired delay time so that the first bit of the data signal is synchronized with the second bit of the data signal.

43. (Currently Amended) In a cross link multiplexer bus configured to convey a data signal in which a character is represented by a first bit of the data signal and a second ~~bit,~~ bit of the data signal, a method for synchronizing the first bit and the second bit, comprising the steps of:

(1) determining a first time for the first bit of the data signal to be conveyed via a first interconnect from a first cross link multiplexer to a second cross link multiplexer when a first series of delay buffers is bypassed;

(2) determining a second time for the second bit of the data signal to be conveyed via a second interconnect from the first cross link multiplexer to the second cross link multiplexer when a second series of delay buffers is bypassed, the second time greater than the first time;

(3) determining a desired delay time for the first bit so that the first bit of the data signal is synchronized with the second ~~bit;~~ bit of the data signal; and

(4) aligning the first series of delay buffers to increase the first time by the desired delay time so that the first bit of the data signal is synchronized with the second ~~bit;~~ bit of the data signal;

wherein said aligning step comprises the steps of:

configuring the first series of delay buffers so that the first bit of the data signal is conveyed through a first delay buffer of the first series of delay buffers; and

configuring the first series of delay buffers so that the first bit of the data signal bypasses a second delay buffer of the first series of delay buffers.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 1, 7, 13, 17-19, 24, 30, 32, 37, 39, 41 and 43 are allowed.

The prior art discloses a network with plurality of cross link multiplexers, wherein the multiplexers have origin and destination ports for transceiving data signals accordingly. The multiplexers further have a plurality of interconnects to couple the adjacent cross link multiplexers.

The prior art however fails to disclose plurality of cross link multiplexers having plurality of interconnects wherein a first interconnect is configured to convey a first bit of a number of bits of the data signal and a second interconnect is configured to convey a second bit of said number of bits of said data signal and said first bit remains substantially synchronized with said second bit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAJ K. JAIN whose telephone number is (571)272-3145. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Raj K. Jain/
Primary Examiner, Art Unit 2616
June 16, 2008